material **203**. The upper portion **202***a* of extended trench **202** is lined with dielectric sidewalls **204** and filled with conductive material **205**. Dielectric material **203** and sidewalls **204** can be silicon dioxide, and conductive material **205** can be doped polysilicon. Conductive material **205** insulated by dielectric material **203** and sidewalls **204** serves as an electrode for a gate region **206** in the upper portion of extended trench **202**.

On one side of extended trench **202** is a P-well region **207** overlying an N-drain zone **208**. Disposed within P-well region **207** at upper surface **209** is a heavily doped P+ body region **210** and a heavily doped N+ source region **211**. On the other side of extended trench **202** is an extended P-zone **212**. Extended trench **202** separates extended zone **212** from drain zone **208**, which are of opposite conduction types. An interlevel dielectric layer **213** is formed over gate region **206**, source region **211**, and extended P-zone **212**. Contact openings **214** enable metal layer **215** to contact body and source regions **210** and **211**, respectively. The rear side **216** of substrate **201** serves as a drain.

Extended P-zone **212** serves to deplete charge when blocking voltage is applied, allowing a much higher conductivity material to be used for drain construction and thereby reducing the on-resistance of the device and improving its efficiency. Dielectric material **203** in bottom trench portion **202***b*, which can beneficially be narrower than upper trench portion **202***a*, prevents lateral diffusion of dopants from extended P-zone **212** into N-drain zone **208**. Extended P-zone **212**, which is thus self-aligned with gate region **206**, is shorted to source region **211** by metal layer **215**. Self-alignment allows the use of structure **200** for making high density devices with blocking voltage capabilities well below 100 V. Since dielectric material **203** serves only as a barrier to dopant diffusion, its quality is not important to the performance of device **200**, which would still function even if zones **208** and **212** were electrically shorted through dielectric material **203**. When device **200** is in the blocking state, zones **208** and **212** will contribute charges with opposite signs, but the induced fields in both zones will cancel out. This allows the use of much higher doping for extended P-zone **212** and particularly for N-drain zone **208**. Current flowing through drain zone **208** thereby undergoes a much lower resistance drop, which in turn reduces the device overall on-resistance and improves its efficiency.

Although the described device is an N-channel silicon device, the present invention can also be applied to other devices and other semiconductor materials and dopants. For example, the described conduction types can be reversed, N for P and P for N. The described device is a power MOSFET, but the present invention is contemplated as applying to all MOS-gated devices such as, for example, IGBTs and MCTs.

A process for making MOS-gated device **200** of the present invention is schematically depicted in FIGS. 2A–D. As shown in FIG. 2A, extended trench **202** is etched into upper layer **201***a* of substrate **201** and substantially filled with dielectric material **203***a*, preferably oxide. A planarization etch step can be used to planarize the oxide **203***a* with upper surface **209** of upper layer **201***a*. A P-dopant is selectively implanted, using standard photolithography techniques, on one side of trench **202**. High temperature diffusion drives the dopant deep into layer **201***a*, thereby forming extended P-zone **212**, as depicted in FIG. 2B.

Dielectric layer **203***a* is recessed below upper surface **209** to a selected depth using dry etching techniques, leaving thick oxide layer **203** in the bottom portion of trench **202**. Dielectric oxide sidewalls **204** are formed in the upper portion of trench **202**, which is then substantially filled with conductive polysilicon **205**, as shown in FIG. 2C. P-well region **207** is implanted into upper layer **201***a* on the side of trench opposite that of extended P-zone **212**, and P+ body region **210** and N+ source region **211** are implanted into well region **207**. Deposition of interlevel dielectric layer **213** and metal layer **215** and formation of contact openings **214** completes the fabrication of device **200**, as depicted in FIG. 2D.

Variations of the described specific process flow are contemplated as being within the present invention. The sequence of trench creation, implantation and etch, for example, can be altered without affecting the final device function and layout.

Although the embodiment described above is an MOS power device, one skilled in the art may adapt the present invention to other devices, including insulated gate bipolar transistors and MOS-controlled thyristors.

The invention has been described in detail for the purpose of illustration, but it is understood that such detail is solely for that purpose, and variations can be made therein by those skilled in the art without departing from the spirit and scope of the invention, which is defined by the following claims.

What is claimed:

1. A trench MOS-gated device comprising:

a substrate including an upper layer, said substrate comprising doped monocrystalline semiconductor material of a first conduction type;

an extended trench in said upper layer, said trench having a bottom portion filled with a dielectric material, said material forming a dielectric layer in said bottom portion of said trench, said trench further having an upper portion lined with a dielectric material and substantially filled with a conductive material, said filled upper portion of said trench forming a gate region;

a doped extended zone of a second opposite conduction type extending from an upper surface into said upper layer only on one side of said trench;

a doped well region of said second conduction type overlying a drain zone of said first conduction type in said upper layer on the opposite side of said trench, said drain zone being substantially insulated from said extended zone by said dielectric layer in said bottom portion of said trench;

a heavily doped source region of said first conduction type and a heavily doped body region of said second conduction type disposed at said upper surface in said well region only on the side of said trench opposite said doped extended zone;

an interlevel dielectric layer on said upper surface overlying said gate and source regions; and

a metal layer overlying said upper surface and said interlevel dielectric layer, said metal layer being in electrical contact with said source and body regions and said extended zone.

2. The device of claim **1** further comprising:

a doped drain zone of said first conduction type extending through said upper layer and into said substrate beneath said well region and said extended zone.

3. The device of claim **2** further comprising:

a heavily doped drain zone of said first conduction type disposed at a lower surface of said substrate.

4. The device of claim **1** wherein said doped extended zone extends into said upper layer to a depth substantially equal to the depth of the bottom of said trench.